X2-10GB-T

The X2-10GB-T is programmed to be fully compatible and functional with all intended Cisco Series switching devices. This X2 transceiver is designed for 10G Ethernet applications and is compliant with the X2 Multi-Source Agreement (MSA) Specification. This module is designed for CAT6A/CAT7 copper cable up to 100 meters.

Compliance:

- IEEE 802.3aN
- 10GBASE-T
- X2 MSA
- RoHS

Applications:

- 10GBd Ethernet

Features:

- Up to 10 GBd bi-directional bit rates
- XAUI electrical interface: 4 lanes @ 3.125 GBd
- Built-in PRBS and jitter test pattern generators
- Hot Z-pluggable
- Up to 100m over CAT6A/CAT7 copper cable
- Adaptable 5V / 3.3V / 1.2V power supply
- Operating Case Temperature: C-Temp: 0° to 70°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Type	Max	Unit	Remarks
Storage Ambient Temperature	T_S	-40		85	° C	
Supply Voltage (5V)	V_5	0		5.3	V	
Supply Voltage (3.3V)	V_3	0		3.6	V	
Supply Voltage (APS)	V_{APS}	0		1.5	V	

General Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Total Power Consumption	P		4.5	5	W	
Supply Voltage (5V)	V_{CC5}	4.75	5	5.25	V	Operating Env
Supply Voltage (+3.3V)	V_{CC3}	3.14	3.3	3.47	V	Operating Env
Supply Voltage (APS)	V_{CCAPS}	1.14	1.2	1.26	V	Operating Env
Supply Current (5V)	I_{CC5}		220	250	mA	
Supply Current (+3.3V)	I_{CC3}		600	650	mA	
Supply Current (APS)	I_{CCAPS}		1000	1100	mA	

MDI Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Signal Speed			10.3125		Gbps	
Length			100		M	CAT6A/CAT7

XAUI Characteristics - Transmitter

Parameter	Symbol	Min	Type	Max	Unit	Remarks
Baud Rate	BR_{XAUI_IN}		3.125		GBd	
Baud Rate Tolerance	BR_{TOL_XAUI}	-100		100	ppm	
Differential Input Impedance	Z_{IN_XAUI}	80	100	120	Ω	
Differential Return Loss	RL_{IN}	10			dB	100MHz to 2.5GHz
Input Differential Skew	T_{IN_SKEW}			75	ps	Crossing Point
Deterministic Jitter	J_{XAUI_DJ}			0.17	UI	
Total Jitter	J_{XAUI_TJ}			0.35	UI	

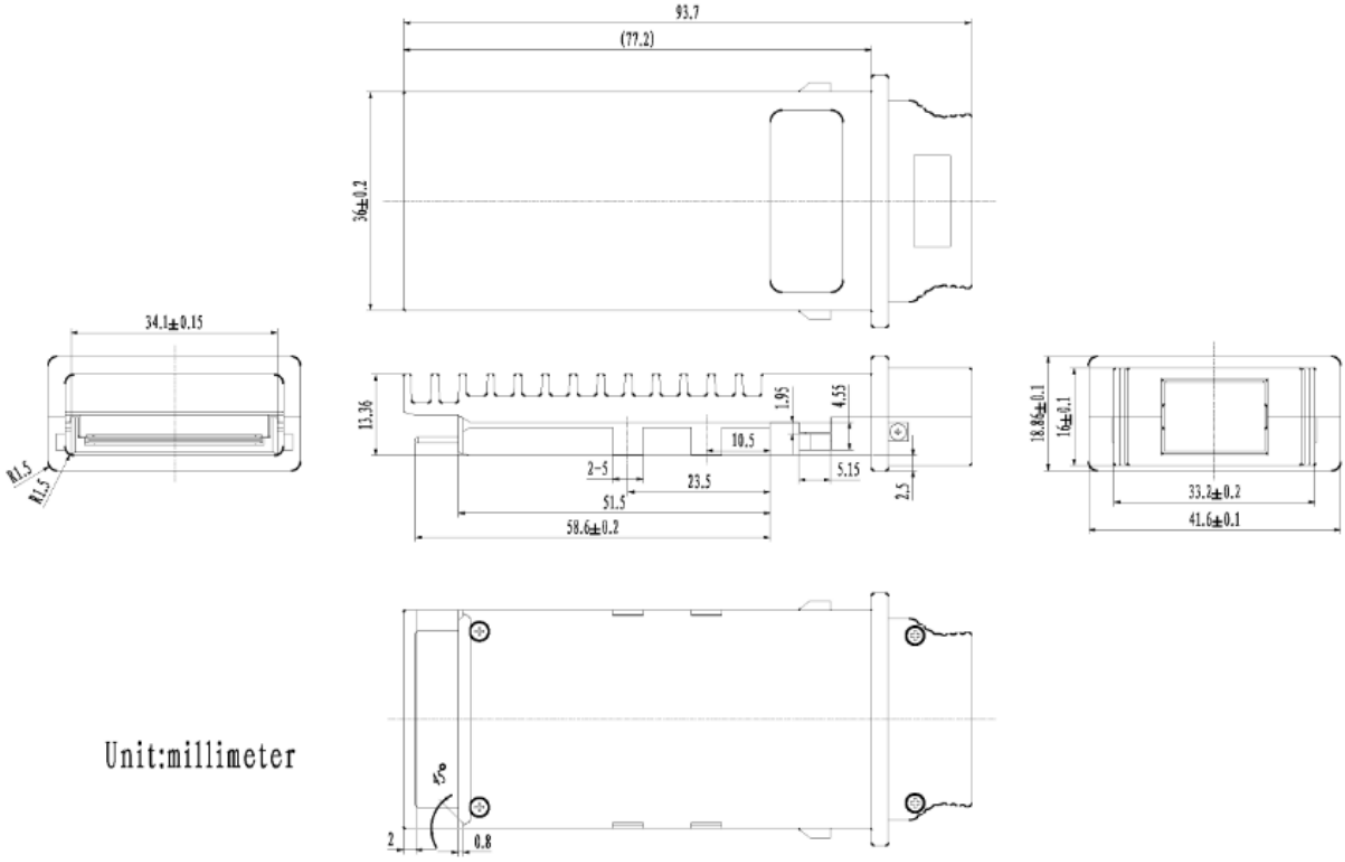
XAUI Characteristics - Receiver

Parameter	Symbol	Min	Type	Max	Unit	Remarks
Baud Rate	BR_{XAUI_OUT}		3.125		GBd	
Baud Rate Variation	BR_{XAUI_VAR}	-100		100	ppm	
XAUI Eye Mask	**According to IEEE 802.3an**					
Output Differential Skew	T_{OUT_SKEW}			15		
Differential Input Impedance	Z_{OUT_XAUI}	80	100	120		
Differential Return Loss	RL_{OUT}	10			dB	100MHz to 2.5GHz
Deterministic Jitter	DJ_{XAUI}			0.17	UI	Near-End No Pre-Equalization
Total Jitter	TJ_{XAUI}			0.35	UI	

MDIO Characteristics

Parameter	Symbol	Min	Type	Max	Unit	Remarks
MDIO Data Hold Time	T_{HOLD}	10			ns	
MDIO Data Hold Time	T_{SU}	10			Ns	
MDC Clock Rate	F_{MAX}			2.5	MHz	

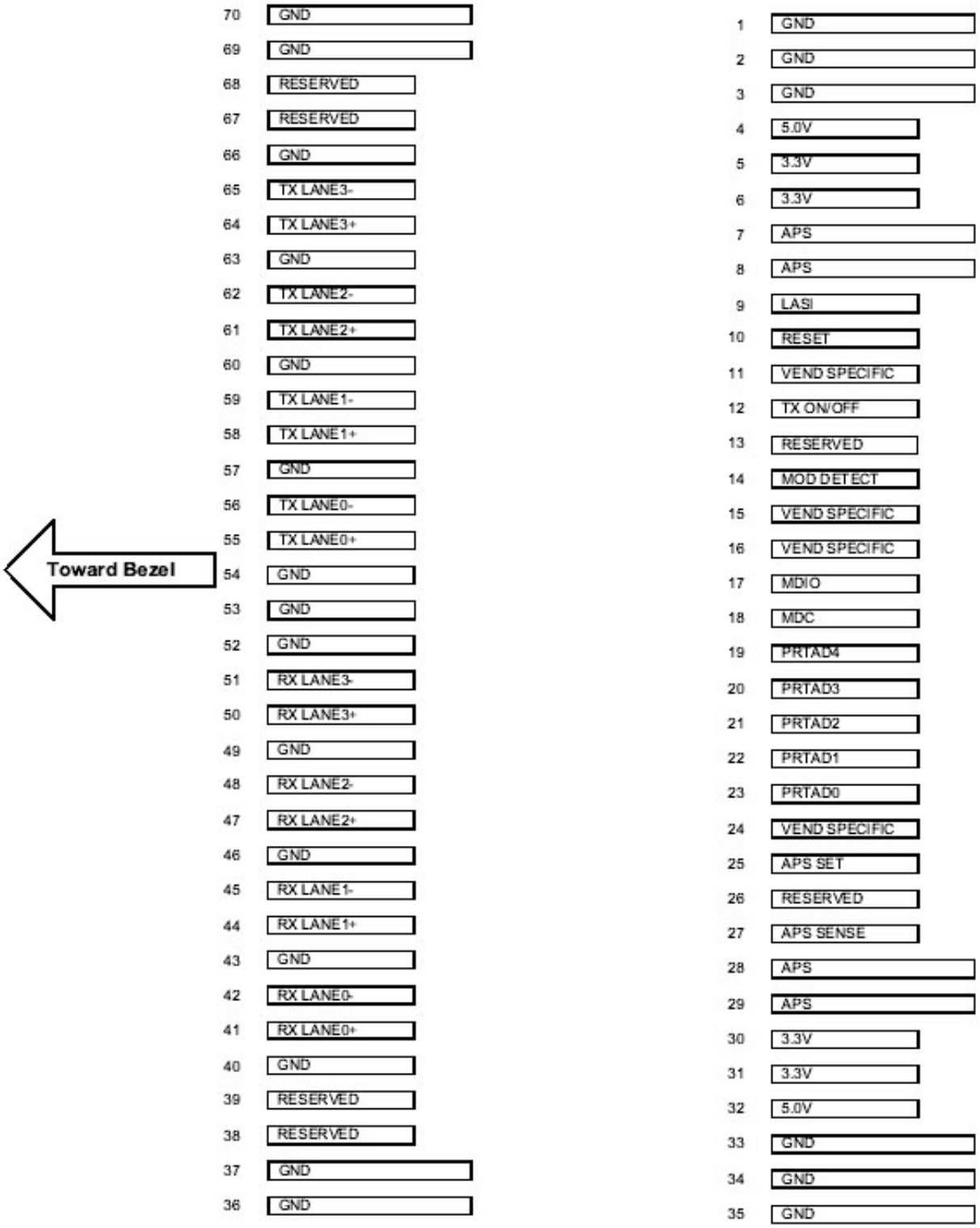
Dimensions



Unit:millimeter

ALL DIMENSIONS ARE ±2.0mm UNLESS OTHERWISE SPECIFIED

Electrical Pad Layout



Pin Assignment - Pin 1 to Pin 35:

PIN #	Symbol	I/O	Logic	Description
1	GND	I	Supply	Electrical ground
2	GND	I	Supply	Electrical ground
3	GND	I	Supply	Electrical ground
4	5.0V	I	Supply	Power
5	3.3V	I	Supply	Power
6	3.3V	I	Supply	Power
7	APS	I	Supply	Adaptive Power Supply
8	APS	I	Supply	Adaptive Power Supply
9	LASI	O	Open Drain	Link Alarm Status Interrupt. 10-22k ohm pull up on host
10	RESET	I	1.2V CMOS	TX OFF when MDIO RESET
11	VEND SPECIFIC			Vendor Specific Pin. Leave unconnected
12	TX ON/OFF	I	1.2V CMOS	Transmitter ON/OFF
13	RESERVED			Reserved
14	MOD DETECT	O		Pulled low inside module through 1k ohm
15	VEND SPECIFIC			Vendor Specific Pin. Leave unconnected
16	VEND SPECIFIC			Vendor Specific Pin. Leave unconnected
17	MDIO	I/O	Open Drain	Management Data IO
18	MDC	I	1.2V CMOS	Management Data Clock
19	PRTAD4	I	1.2V CMOS	Port Address bit 4 (Low=0)
20	PRTAD3	I	1.2V CMOS	Port Address bit 3 (Low=0)
21	PRTAD2	I	1.2V CMOS	Port Address bit 2 (Low=0)
22	PRTAD1	I	1.2V CMOS	Port Address bit 1 (Low=0)
23	PRTAD0	I	1.2V CMOS	Port Address bit 0 (Low=0)
24	VEND SPECIFIC			Vendor Specific Pin. Leave unconnected
25	APS SET	O		Feedback output for APS
26	RESERVED			Reserved for Avalanche Photodiode use
27	APS SENSE	O	Analog	APS Sense Connection
28	APS	I	Supply	Adaptive Power Supply
29	APS	I	Supply	Adaptive Power Supply
30	3.3V	I	Supply	Power
31	3.3V	I	Supply	Power
32	5.0V		Supply	Power
33	GND	I	Supply	Electrical Ground
34	GND	I	Supply	Electrical Ground
35	GND	I	Supply	Electrical Ground

Pin Assignment - Pin 36 to Pin 70:

PIN #	Symbol	I/O	Logic	Description
36	GND	I	Supply	Electrical ground
37	GND	I	Supply	Electrical ground
38	RESERVED			Reserved
39	RESERVED			Reserved
40	GND	I	Supply	Electrical ground
41	RX LANE 0+	O	AC	Module XAUI Output Lane 0+
42	RX LANE 0-	O	AC	Module XAUI Output Lane 0-
43	GND	I	Supply	Electrical ground
44	RX LANE 1+	O	AC	Module XAUI Output Lane 1+
45	RX LANE 1-	O	AC	Module XAUI Output Lane 1-
46	GND	I	Supply	Electrical ground
47	RX LANE 2+	O	AC	Module XAUI Output Lane 2+
48	RX LANE 2-	O	AC	Module XAUI Output Lane 2-
49	GND	I	Supply	Electrical ground
50	RX LANE 3+	O	AC	Module XAUI Output Lane 3+
51	RX LANE 3-	O	AC	Module XAUI Output Lane 3-
52	GND	I	Supply	Electrical ground
53	GND	I	Supply	Electrical ground
54	GND	I	Supply	Electrical ground
55	TX LANE 0+	O	AC	Module XAUI Input Lane 0+
56	TX LANE 0-	O	AC	Module XAUI Input Lane 0-
57	GND	I	Supply	Electrical ground
58	TX LANE 1+	O	AC	Module XAUI Input Lane 1+
59	TX LANE 1-	O	AC	Module XAUI Input Lane 1-
60	GND	I	Supply	Electrical ground
61	TX LANE 2+	O	AC	Module XAUI Input Lane 2+
62	TX LANE 2-	O	AC	Module XAUI Input Lane 2-
63	GND	I	Supply	Electrical ground
64	TX LANE 3+	O	AC	Module XAUI Input Lane 3+
65	TX LANE 3-	O	AC	Module XAUI Input Lane 3-
66	GND	I	Supply	Electrical ground
67	RESERVED			Reserved
68	RESERVED			Reserved
69	GND	I	Supply	Electrical Ground
70	GND	I	Supply	Electrical Ground

Remarks

1. IEEE standard 802.3 IEEE Standard Department, 2008
2. X2 Multi-Source Agreement (MSA)